Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1 (Currently amended). A tuning circuit comprising:

a voltage controlled oscillator for generating a first clock signal comprising:

an inductive element;

a variable capacitive element coupled to the inductive element;

a bank of switched capacitors coupled to the inductive element and the variable capacitive element;

a frequency divider for generating a second clock signal responsive to the first clock signal ~~an~~ and a ~~predetermined~~ selected divisor;

frequency control circuitry for ~~controlling~~ adjusting a control voltage to the variable capacitive element responsive to a frequency difference between the ~~first and~~ second clock signal and a reference signal to oscillate the first clock signal at a desired frequency ~~signals~~; and

logic circuitry for calibrating the voltage controlled oscillator to a frequency range inclusive of a new desired frequency responsive to a change in the divisor by:

performing a coarse search at a predetermined control voltage to determine an initial control word ~~determining an initial control word to configure the bank using a search responsive to a desired frequency~~; and

testing the initial control word to determine ~~determining~~ whether the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word.

2 (Original). The tuning circuit of claim 1 wherein said logic circuitry determines an initial control word to configure the bank by using a search having an accuracy that is greater than or equal to ±1 least significant bit of the initial control word.

3 (Currently amended). The tuning circuit of claim 1 wherein the logic circuitry tests the initial control word ~~determines whether the initial control word remains the same~~ by comparing the desired frequency to upper and lower bounds of a frequency range for the voltage controlled oscillator while configured according to the initial control word.

4 (Currently amended). The tuning circuit of claim 3 wherein the logic circuitry determines the initial control word using fast comparisons between an actual frequency at the predetermined control voltage and the desired frequency and determines whether the initial control word should remain the same by using more precise comparisons between the actual frequency and the desired frequency.

5 (Currently amended). The tuning circuit of claim 1 wherein the logic circuitry tests the initial control word ~~determines whether the initial control word remains the same~~ by determining whether the difference between the desired frequency and an actual frequency for the voltage controlled oscillator while configured according to the initial control word is within a predetermined threshold.

6 (Original). The tuning circuit of claim 5 wherein an indication of the actual frequency is determined by counting clock cycles from the voltage controlled oscillator in a frequency divider circuit.

7 (Currently amended). A method of calibrating a voltage controlled oscillator having an LC tank with an inductive element, a variable capacitive element coupled to the inductive element, where the capacitance of the variable capacitive element is controlled by a control voltage, and a bank of switched capacitors coupled to the inductive element and the variable capacitive element, comprising the steps of:

determining an initial control word to configure the bank using a search at a predetermined control voltage; ~~responsive to~~ a desired frequency; and

~~enabling a set switched capacitors in the bank responsive to the initial control word;~~

testing the initial control word to determine whether the frequency range produced by the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word.

~~comparing an output frequency from the voltage controlled oscillator with the desired frequency; and~~

~~determining whether the initial control word should either remain the same or change to an adjacent control word.~~

8 (Original). The method of claim 1 wherein said step of determining an initial control word comprises the step of determining an initial control word to configure the bank by using a search having an accuracy that is greater than or equal to ±1 least significant bit of the initial control word.

9 (Currently amended). The method of claim 7 wherein the step of testing the initial control word ~~determining whether the initial control word remains the same~~ comprises the step of comparing the desired frequency to upper and lower bounds of a frequency range for the voltage controlled oscillator while configured according to the initial control word.

10 (Currently amended). The method of claim 9 wherein the step of determining the initial control word comprises the step of using fast comparisons between an actual frequency at the predetermined control voltage and the desired frequency and wherein the step of determining whether the initial control word should remain the same comprises the step of using more precise comparisons between the actual frequency and the desired frequency.

11 (Currently amended). The method of claim 7 wherein the step of testing the initial control word ~~determining whether the initial control word remains the same~~ comprises the step of determining whether the difference between the desired

frequency and an actual frequency for the voltage controlled oscillator while configured according to the initial control word is within a predetermined threshold.

12 (Original). The method of claim 7 wherein the step of determining whether the difference between the desired frequency and an actual frequency is within a predetermined threshold comprises the step of calculating an indication of the actual frequency by counting clock cycles from the voltage controlled oscillator in a frequency divider circuit.